专业电机芯片，内部集成 32-bit Cortex-M4 处理器

- 工作电压范围：2.5～5.5V
- 工作温度范围：-40℃～105℃
- 32-bit Cortex-M4 CPU 内核
  - 最高 80 MHz 工作频率
  - 单周期乘法和硬件除法
  - FPU
- 存储器
  - 256K Flash
  - 20 K SRAM
  - 40 K CCM
  - AMPU
- 时钟，复位和电源管理
  - 2.0 ～5.5 V 供电和 I/O 引脚
  - POR, PDR, PVD
  - 4-16 MHz 晶体振荡器
  - 内建出厂校准的 8MHz 的 RC 振荡器
  - 内建出厂校准的 40KHz 的 RC 振荡器
  - 产生 CPU 时钟的 PLL
- 低功耗
  - 睡眠，待机和停机模式
- 3×12 位 ADC, 1MSPS
  - 1×10 通道 , 1×7 通道, 1×10 通道
  - 通过可编程增益放大器放大输入信号
  - 转换范围: 0 ～AVCC
  - 温度传感器
- 2×DMA
  - 1×7 通道 DMA1, 1×8 通道 DMA3
  - 支持的外设： Timers, ADC, SPIs, I^2Cs , USARTs
- 67 个快速 I/O 口
  - 53/67 I/Os，均可映像到 16 个外部中断
- 调试模式
  - 串行单线调试(SWD) 和 JTAG 接口
- 3×CMP
- 1×OPA
- 2×PGA
- 1×CRV
  - 双电平，32 个档位
  - 被用作比较器的参考电压源
- MEII 电机协同处理器
  - PID/CORDIC/SVPWM
- 9 个定时器
  - 3 个 16 位定时器，每个定时器有多达 4 个用于输入捕获/输出比较/PWM 或脉冲计数的通道和增量编码器输入
  - 3 个 16 位 6 通道带死区控制和紧急刹车，用于电机控制的 PWM 高级控制定时器。
  - 2 个看门狗定时器 (独立和窗口型)
  - 系统时间定时器：24 位自减型计数器
- 8 个通信接口
  - 2×I^2C 接口 (支持 SMBus/PMBus)
  - 3×USARTs
  - 2×SPIs
  - 1×CAN 接口(2.0B 主动)
- CRC 计算单元：96 位芯片唯一代码
- 采用绿色封装：
LQFP64, LQFP80

版本历史

版本号	改动内容
V0.1	创建
V0.2	封面中文化修正
V0.3	新增封装图，简介内容更正

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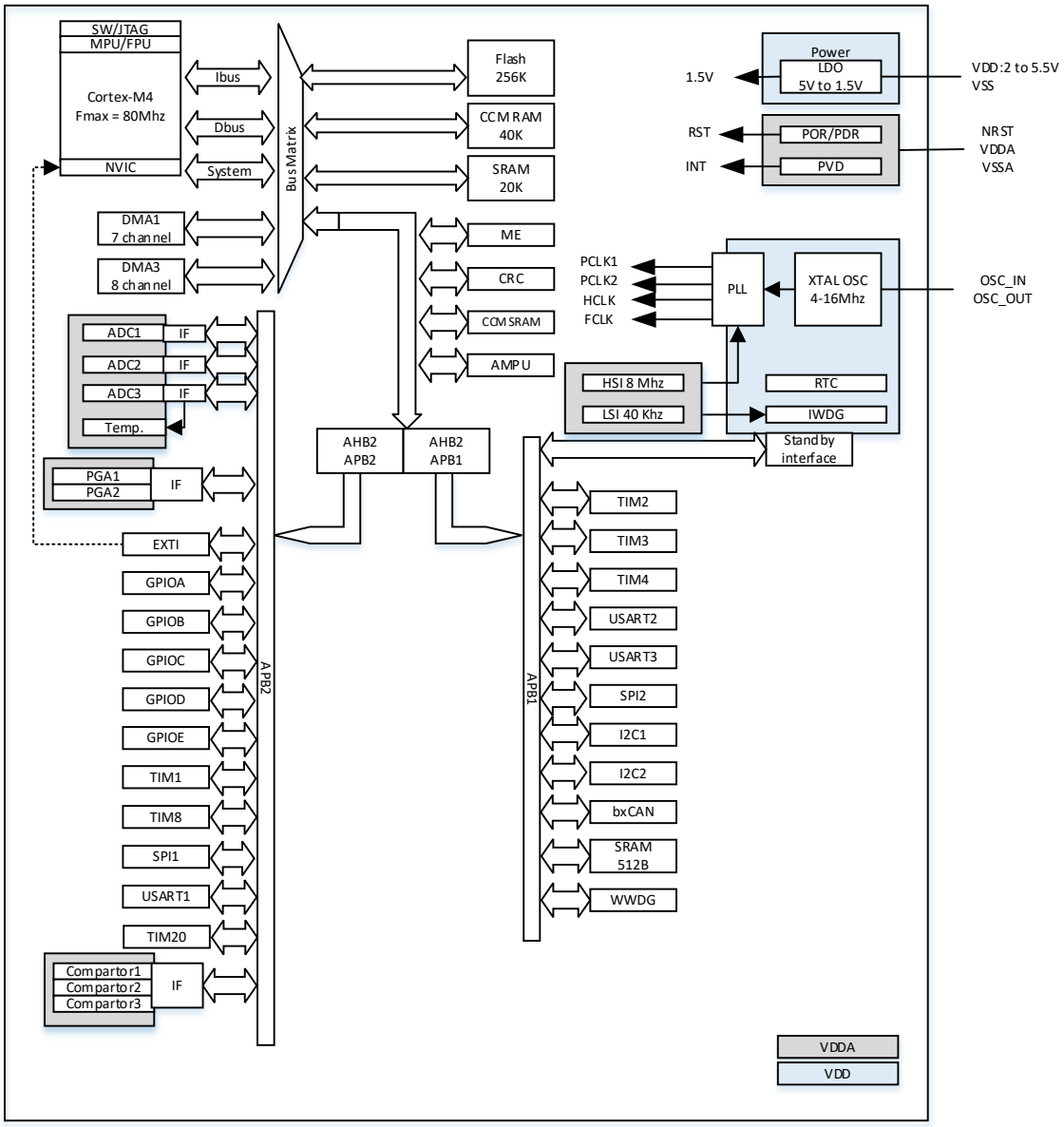
简介

RX32S50 系列是高性能、低功耗、多功能马达专用 32 bit Cortex M4 MCU 芯片，工作温度范围 -40~105℃，工作电压 2.5-5.5V。芯片针对双电机应用集成高级定时器、三个 12bit SAR ADC、可满足单电阻/双电阻采样的不同需求芯片整合了内部高频/低频 RC、可编成增益放大器、 比较器，在使用上能更节省布局空间，更节省成本。

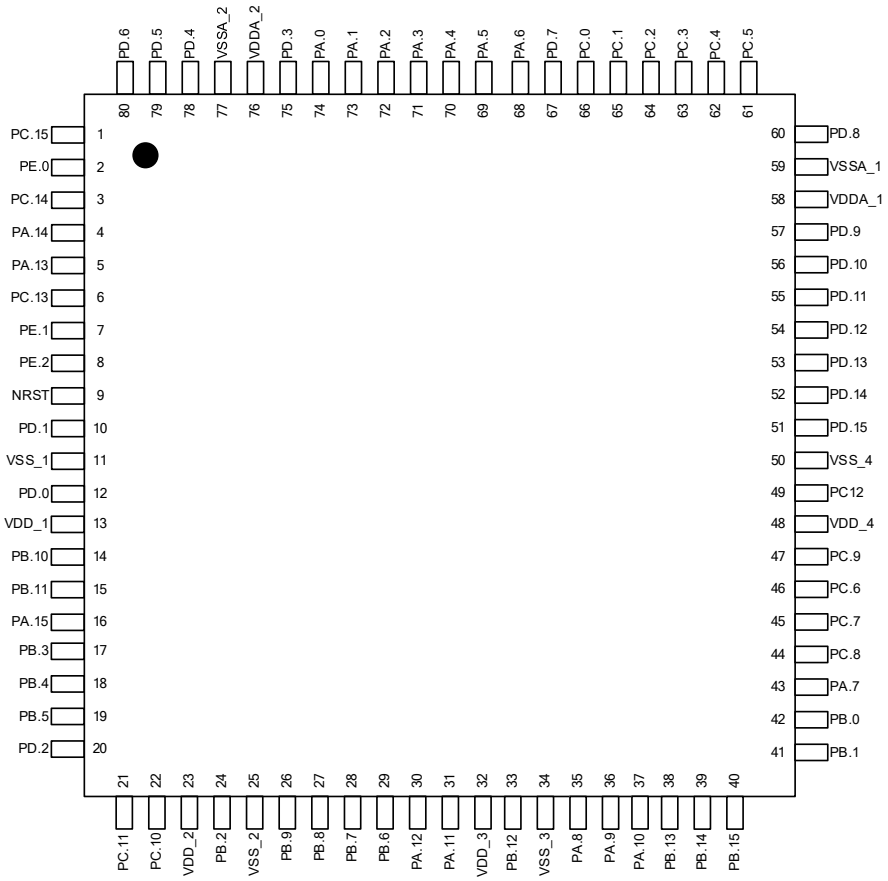
- 工作电压范围：2.5V～5.5V
- 工作温度范围：-40℃～105℃
- 采用 Cortex-M4 的处理器、256K Flash、20K SRAM、40K CCM
- 高速度：CPU 最高工作频率达到 80MHz
- 采用绿色封装：LQFP64；LQFP80；

系统框图

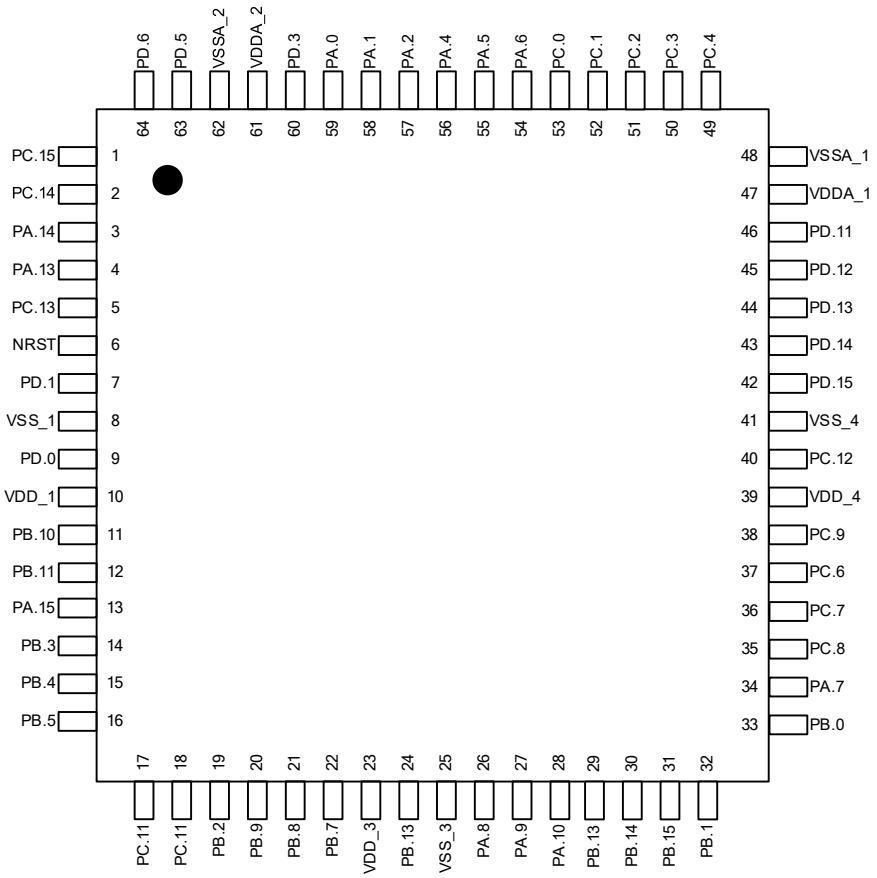

SW/JTAG
MPU/FPU
Cortex-M4
Fmax = 80Mhz
NVIC
Ibus
Dbus
System
Bus Matrix
Flash
256K
CCM RAM
40K
SRAM
20K
DMA1
7 channel
DMA3
8 channel
ME
CRC
CCM SRAM
AMPU
Power
LDO
5V to 1.5V
1.5V
VDD:2 to 5.5V
VSS
RST
INT
POR/PDR
PVD
NRST
VDDA
VSSA
PCLK1
PCLK2
HCLK
FCLK
PLL
XTAL OSC
4-16Mhz
OSC_IN
OSC_OUT
HSI 8 Mhz
LSI 40 Khz
RTC
IWDG
Stand by
interface
ADC1
ADC2
ADC3
Temp.
IF
PGA1
PGA2
AHB2
APB2
AHB2
APB1
EXTI
GPIOA
GPIOB
GPIOC
GPIOD
GPIOE
TIM1
TIM8
SPI1
USART1
TIM20
Compartor1
Compartor2
Compartor3
APB2
APB1
TIM2
TIM3
TIM4
USART2
USART3
SPI2
I2C1
I2C2
bxCAN
SRAM
512B
WWDG
VDDA
VDD

引脚排列

LQFP80


PC.15 1
PE.0 2
PC.14 3
PA.14 4
PA.13 5
PC.13 6
PE.1 7
PE.2 8
NRST 9
PD.1 10
VSS_1 11
PD.0 12
VDD_1 13
PB.10 14
PB.11 15
PA.15 16
PB.3 17
PB.4 18
PB.5 19
PD.2 20
21 PC.11
22 PC.10
23 VDD_2
24 PB.2
25 VSS_2
26 PB.9
27 PB.8
28 PB.7
29 PB.6
30 PA.12
31 PA.11
32 VDD_3
33 PB.12
34 VSS_3
35 PA.8
36 PA.9
37 PA.10
38 PB.13
39 PB.14
40 PB.15
41 PB.1
42 PB.0
43 PA.7
44 PC.8
45 PC.7
46 PC.6
47 PC.9
48 VDD_4
49 PC12
50 VSS_4
51 PD.15
52 PD.14
53 PD.13
54 PD.12
55 PD.11
56 PD.10
57 PD.9
58 VDDA_1
59 VSSA_1
60 PD.8
61 PC.5
62 PC.4
63 PC.3
64 PC.2
65 PC.1
66 PC.0
67 PD.7
68 PA.6
69 PA.5
70 PA.4
71 PA.3
72 PA.2
73 PA.1
74 PA.0
75 PD.3
76 VDDA_2
77 VSSA_2
78 PD.4
79 PD.5
80 PD.6

LQFP64

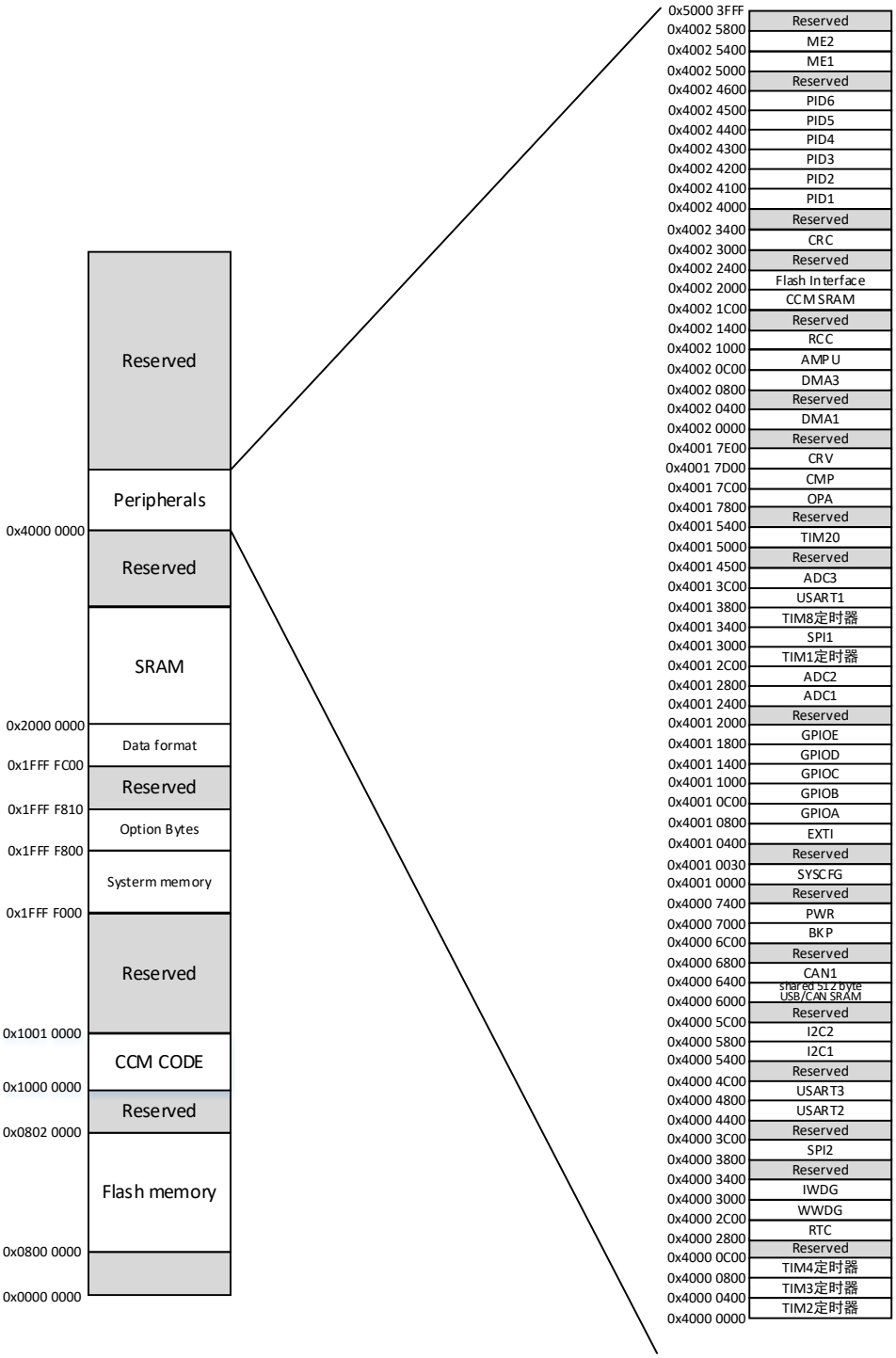

PD.6 64
PD.5 63
VSSA_2 62
VDDA_2 61
PD.3 60
PA.0 59
PA.1 58
PA.2 57
PA.4 56
PA.5 55
PA.6 54
PC.0 53
PC.1 52
PC.2 51
PC.3 50
PC.4 49
PC.15 1
PC.14 2
PA.14 3
PA.13 4
PC.13 5
NRST 6
PD.1 7
VSS_1 8
PD.0 9
VDD_1 10
PB.10 11
PB.11 12
PA.15 13
PB.3 14
PB.4 15
PB.5 16
48 VSSA_1
47 VDDA_1
46 PD.11
45 PD.12
44 PD.13
43 PD.14
42 PD.15
41 VSS_4
40 PC.12
39 VDD_4
38 PC.9
37 PC.6
36 PC.7
35 PC.8
34 PA.7
33 PB.0
17 PC.11
18 PC.11
19 PB.2
20 PB.9
21 PB.8
22 PB.7
23 VDD_3
24 PB.13
25 VSS_3
26 PA.8
27 PA.9
28 PA.10
29 PB.13
30 PB.14
31 PB.15
32 PB.1

引脚定义

80 PIN	标识	引脚类型	Main Fuction (after reset)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Analog		
1	PC15	I/O	PC15									ADC1_IN6		
2	PE0	I/O	PE0			TIM20_CH4	USART2_CK					ADC1_IN7		
3	PC14	I/O	PC14/WKUP									ADC1_IN8		
4	PA14	I/O	JTCK/SWCLK	JTCK/SWCLK										
5	PA13	I/O	JTMS/SWDIO	JTMS/SWDIO										
6	PC13	I/O	PC13/TAMPER-RTC											
7	PE1	I/O	PE1			TIM20_CH5	USART2_TX							
8	PE2	I/O	PE2			TIM20_CH6	USART2_RX							
9	NRST	I												
10	PD1	I/O	OSC_OUT									OSC_OUT		
11	VSS_1	G												
12	PD0	I/O	OSC_IN									OSC_IN		
13	VDD_1	P												
14	PB10	I/O	PB10		TIM2_CH3		USART1_TX		I2C2_SCL					
15	PB11	I/O	PB11		TIM2_CH4		USART1_RX		I2C2_SDA					
16	PA15	I/O	JTDI	JTDI	TIM2_CH1_ETR			SPI1_NSS						
17	PB3	I/O	JTDO	JTDO/TRACESWO	TIM2_CH2		USART1_RX	SPI1_SCK						
18	PB4	I/O	JNTRST	JNTRST	TIM3_CH1			SPI1_MISO						
19	PB5	I/O	PB5		TIM3_CH2		USART1_TX	SPI1_MOSI	I2C1_SMBAI					
20	PD2	I/O	PD2		TIM3_ETR									
21	PC11	I/O	PC11		TIM3_CH4		USART3_RX							
22	PC10	I/O	PC10		TIM3_CH3		USART3_TX							
23	VDD_2	P												
24	PB2	I/O	PB2											
25	VSS_2	G												
26	PB9	I/O	PB9		TIM4_CH4				I2C1_SDA	CANTX				
27	PB8	I/O	PB8		TIM4_CH3				I2C1_SCL	CANRX				
28	PB7	I/O	PB7		TIM4_CH2		USART3_RX		I2C1_SDA					
29	PB6	I/O	PB6		TIM4_CH1		USART3_TX		I2C1_SCL					
30	PA12	I/O	PA12			TIM1_ETR	USART1_RTS			CANTX				
31	PA11	I/O	PA11				USART1_CTS			CANRX				
32	VDD_3	P												
33	PB12	I/O	PB12			TIM1_BKIN	USART1_CK	SPI2_NSS	I2C2_SMBAI	TIM8_ETR				
34	VSS_3	G												
35	PA8	I/O	PA8	MCO		TIM1_CH1								
36	PA9	I/O	PA9			TIM1_CH2								
37	PA10	I/O	PA10			TIM1_CH3								
38	PB13	I/O	PB13			TIM1_CH1N				TIM8_CH6				
39	PB14	I/O	PB14			TIM1_CH2N				TIM8_CH5				
40	PB15	I/O	PB15			TIM1_CH3N				TIM8_CH4				
41	PB1	I/O	PB1			TIM1_CH4				TIM8_CH3N				
42	PB0	I/O	PB0			TIM1_CH5				TIM8_CH2N				
43	PA7	I/O	PA7			TIM1_CH6				TIM8_CH1N				
44	PC8	I/O	PC8							TIM8_CH3				
45	PC7	I/O	PC7							TIM8_CH2				
46	PC6	I/O	PC6							TIM8_CH1				
47	PC9	I/O	PC9		TIM3_CH4	TIM8_BKIN				TIM8_CH4				
48	VDD_4	P												
49	PC12	I/O	PC12			TIM20_BKIN	USART3_CK							
50	VSS_4	G												
51	PD15	I/O	PD15		TIM4_CH4	TIM20_CH1		SPI2_NSS						
52	PD14	I/O	PD14		TIM4_CH3	TIM20_CH2	USART2_CK	SPI2_SCK						
53	PD13	I/O	PD13		TIM4_CH2	TIM20_CH3	USART2_TX	SPI2_MOSI						
54	PD12	I/O	PD12		TIM4_CH1	TIM20_CH1N	USART2_RX	SPI2_MISO						
55	PD11	I/O	PD11		TIM2_CH4	TIM20_CH2N	USART2_RTS							
56	PD10	I/O	PD10		TIM2_CH3	TIM20_CH3N	USART2_CTS							
57	PD9	I/O	PD9									ADC3_IN0		
58	VDDA_1	P												
59	VSSA_1	G												
60	PD8	I/O	PD8									ADC3_IN1		
61	PC5	I/O	PC5									ADC3_IN2		
62	PC4	I/O	PC4									ADC3_IN3		CMP3_N
63	PC3	I/O	PC3									ADC3_IN4		CMP3_P
64	PC2	I/O	PC2									ADC3_IN5	OPA_O	
65	PC1	I/O	PC1									ADC3_IN6	OPA_N	
66	PC0	I/O	PC0									ADC3_IN7	OPA_P	
67	PD7	I/O	PD7									ADC2_IN5		
68	PA6	I/O	PA6									ADC2_IN4		
69	PA5	I/O	PA5									ADC2_IN3	PGA2_N	CMP2_N
70	PA4	I/O	PA4									ADC2_IN2	PGA2_P	CMP2_P
71	PA3	I/O	PA3									ADC2_IN1		
72	PA2	I/O	PA2									ADC2_IN0		
73	PA1	I/O	PA1									ADC1_IN0	PGA1_N	CMP1_N
74	PA0	I/O	PA0									ADC1_IN1	PGA1_P	CMP1_P
75	PD3	I/O	PD3									ADC1_IN2		
76	VDDA_2	P												
77	VSSA_2	G												
78	PD4	I/O	PD4								CMP1_OUT	ADC1_IN3		
79	PD5	I/O	PD5								CMP2_OUT	ADC1_IN4		
80	PD6	I/O	PD6								CMP3_OUT	ADC1_IN5		

64 PIN	标识	引脚类型	Main Fuction (after reset)	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	Analog		
1	PC15	I/O	PC15									ADC1_IN6		
2	PC14	I/O	PC14/WKUP									ADC1_IN8		
3	PA14	I/O	JTCK/SWCLK	JTCK/SWCLK										
4	PA13	I/O	JTMS/SWDIO	JTMS/SWDIO										
5	PC13	I/O	PC13/TAMPER-RTC											
6	NRST	I												
7	PD1	I/O	OSC_OUT									OSC_OUT		
8	VSS_1	G												
9	PD0	I/O	OSC_IN									OSC_IN		
10	VDD_1	P												
11	PB10	I/O	PB10		TIM2_CH3		USART1_TX		I2C2_SCL					
12	PB11	I/O	PB11		TIM2_CH4		USART1_RX		I2C2_SDA					
13	PA15	I/O	JTDI	JTDI	TIM2_CH1_ETR			SPI1_NSS						
14	PB3	I/O	JTDO	JTDO/TRACESWO	TIM2_CH2		USART1_RX	SPI1_SCK						
15	PB4	I/O	JNTRST	JNTRST	TIM3_CH1			SPI1_MISO						
16	PB5	I/O	PB5		TIM3_CH2		USART1_TX	SPI1_MOSI	I2C1_SMBAI					
17	PC11	I/O	PC11		TIM3_CH4		USART3_RX							
18	PC10	I/O	PC10		TIM3_CH3		USART3_TX							
19	PB2	I/O	PB2											
20	PB9	I/O	PB9		TIM4_CH4				I2C1_SDA	CANTX				
21	PB8	I/O	PB8		TIM4_CH3				I2C1_SCL	CANRX				
22	PB7	I/O	PB7		TIM4_CH2		USART3_RX		I2C1_SDA					
23	VDD_3	P												
24	PB12	I/O	PB12			TIM1_BKIN	USART1_CK	SPI2_NSS	I2C2_SMBAI	TIM8_ETR				
25	VSS_3	G												
26	PA8	I/O	PA8	MCO		TIM1_CH1								
27	PA9	I/O	PA9			TIM1_CH2								
28	PA10	I/O	PA10			TIM1_CH3								
29	PB13	I/O	PB13			TIM1_CH1N				TIM8_CH6				
30	PB14	I/O	PB14			TIM1_CH2N				TIM8_CH5				
31	PB15	I/O	PB15			TIM1_CH3N				TIM8_CH4				
32	PB1	I/O	PB1			TIM1_CH4				TIM8_CH3N				
33	PB0	I/O	PB0			TIM1_CH5				TIM8_CH2N				
34	PA7	I/O	PA7			TIM1_CH6				TIM8_CH1N				
35	PC8	I/O	PC8							TIM8_CH3				
36	PC7	I/O	PC7							TIM8_CH2				
37	PC6	I/O	PC6							TIM8_CH1				
38	PC9	I/O	PC9		TIM3_CH4	TIM8_BKIN				TIM8_CH4				
39	VDD_4	P												
40	PC12	I/O	PC12			TIM20_BKIN	USART3_CK							
41	VSS_4	G												
42	PD15	I/O	PD15		TIM4_CH4	TIM20_CH1		SPI2_NSS						
43	PD14	I/O	PD14		TIM4_CH3	TIM20_CH2	USART2_CK	SPI2_SCK						
44	PD13	I/O	PD13		TIM4_CH2	TIM20_CH3	USART2_TX	SPI2_MOSI						
45	PD12	I/O	PD12		TIM4_CH1	TIM20_CH1N	USART2_RX	SPI2_MISO						
46	PD11	I/O	PD11		TIM2_CH4	TIM20_CH2N	USART2_RTS							
47	VDDA_1	P												
48	VSSA_1	G												
49	PC4	I/O	PC4									ADC3_IN3		CMP3_N
50	PC3	I/O	PC3									ADC3_IN4		CMP3_P
51	PC2	I/O	PC2									ADC3_IN5	OPA_O	
52	PC1	I/O	PC1									ADC3_IN6	OPA_N	
53	PC0	I/O	PC0									ADC3_IN7	OPA_P	
54	PA6	I/O	PA6									ADC2_IN4		
55	PA5	I/O	PA5									ADC2_IN3	PGA2_N	CMP2_N
56	PA4	I/O	PA4									ADC2_IN2	PGA2_P	CMP2_P
57	PA2	I/O	PA2									ADC2_IN0		
58	PA1	I/O	PA1									ADC1_IN0	PGA1_N	CMP1_N
59	PA0	I/O	PA0									ADC1_IN1	PGA1_P	CMP1_P
60	PD3	I/O	PD3									ADC1_IN2		
61	VDDA_2	P												
62	VSSA_2	G												
63	PD5	I/O	PD5								CMP2_OUT	ADC1_IN4		
64	PD6	I/O	PD6								CMP3_OUT	ADC1_IN5		

存储器映射图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Reserved
SRAM
0x2000 0000
Data format
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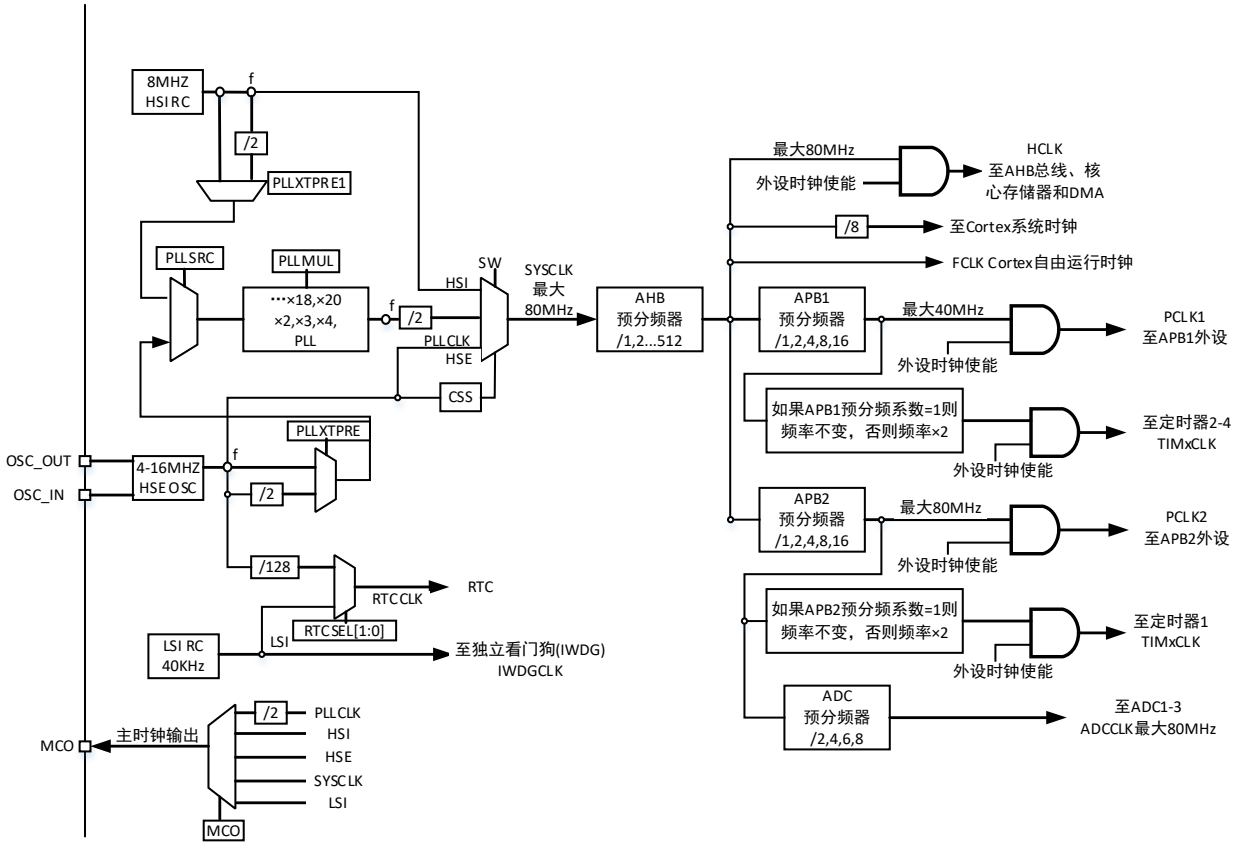
Reserved
0x1FFF F810
Option Bytes
0x1FFF F800
Systerm memory
0x1FFF F000
Reserved
0x1001 0000
CCM CODE
0x1000 0000
Reserved
0x0802 0000
Flash memory
0x0800 0000
0x0000 0000
0x5000 3FFF
Reserved
0x4002 5800
ME2
0x4002 5400
ME1
0x4002 5000
Reserved
0x4002 4600
PID6
0x4002 4500
PID5
0x4002 4400
PID4
0x4002 4300
PID3
0x4002 4200
PID2
0x4002 4100
PID1
0x4002 4000
Reserved
0x4002 3400
CRC
0x4002 3000
Reserved
0x4002 2400
Flash Interface
0x4002 2000
CCM SRAM
0x4002 1C00
Reserved
0x4002 1400
RCC
0x4002 1000
AMPU
0x4002 0C00
DMA3
0x4002 0800
Reserved
0x4002 0400
DMA1
0x4002 0000
Reserved
0x4001 7E00
CRV
0x4001 7D00
CMP
0x4001 7C00
OPA
0x4001 7800
Reserved
0x4001 5400
TIM20
0x4001 5000
Reserved
0x4001 4500
ADC3
0x4001 3C00
USART1
0x4001 3800
TIM8定时器
0x4001 3400
SPI1
0x4001 3000
TIM1定时器
0x4001 2C00
ADC2
0x4001 2800
ADC1
0x4001 2400
Reserved
0x4001 2000
GPIOE
0x4001 1800
GPIOD
0x4001 1400
GPIOC
0x4001 1000
GPIOB
0x4001 0C00
GPIOA
0x4001 0800
EXTI
0x4001 0400
Reserved
0x4001 0030
SYSCFG
0x4001 0000
Reserved
0x4000 7400
PWR
0x4000 7000
BKP
0x4000 6C00
Reserved
0x4000 6800
CAN1
0x4000 6400
shared 512 byte USB/CAN SRAM
0x4000 6000
Reserved
0x4000 5C00
I2C2
0x4000 5800
I2C1
0x4000 5400
Reserved
0x4000 4C00
USART3
0x4000 4800
USART2
0x4000 4400
Reserved
0x4000 3C00
SPI2
0x4000 3800
Reserved
0x4000 3400
IWDG
0x4000 3000
WWDG
0x4000 2C00
RTC
0x4000 2800
Reserved
0x4000 0C00
TIM4定时器
0x4000 0800
TIM3定时器
0x4000 0400
TIM2定时器
0x4000 0000

时钟框图


8MHZ
HSI RC
f
/2
PLLXTPRE1
PLLSRC
PLLMUL
····×18,×20
×2,×3,×4,
PLL
f
/2
SW
HSI
PLLCLK
HSE
SYSCLK
最大
80MHz
CSS
AHB
预分频器
/1,2...512
最大80MHz
外设时钟使能
HCLK
至AHB总线、核
心存储器和DMA
/8
至Cortex系统时钟
FCLK Cortex自由运行时钟
APB1
预分频器
/1,2,4,8,16
最大40MHz
外设时钟使能
PCLK1
至APB1外设
如果APB1预分频系数=1则
频率不变，否则频率×2
外设时钟使能
至定时器2-4
TIMxCLK
APB2
预分频器
/1,2,4,8,16
最大80MHz
外设时钟使能
PCLK2
至APB2外设
如果APB2预分频系数=1则
频率不变，否则频率×2
外设时钟使能
至定时器1
TIMxCLK
ADC
预分频器
/2,4,6,8
至ADC1-3
ADCCLK最大80MHz
PLLXTPRE
OSC_OUT
OSC_IN
4-16MHZ
HSE OSC
f
/2
/128
RTCCLK
RTC
RTCSEL[1:0]
LSI
LSI RC
40KHz
至独立看门狗(IWDG)
IWDGCLK
MCO
主时钟输出
/2
PLLCLK
HSI
HSE
SYSCLK
LSI
MCO

AC/DC 参数

12.1 Absolute maximum ratings

Voltage characteristics				
Symbol	**Ratings**	**Min**	**Max**	**Unit**
VDD - VSS	External main supply voltage (including VDDA and VDD)(1)			V
VIN(2)	Input voltage on five volt tolerant pin			
	Input voltage on any other pin			
$\lvert\triangle V_{DDx}\rvert$	Variations between different VDD power pins			mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins			
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)			KV

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. VIN maximum must always be respected. Refer to Current characteristics for the maximum allowed injected current values.

Current characteristics				
Symbol	**Ratings**	**Condition**	**Max.**	**Unit**
I_{VDD}	Total current into VDD/VDDA power lines (source)(1)	VCC=3.3V		mA
		VCC=5V		
I_{VSS}	Total current out of VSS ground lines (sink)(1)	VCC=3.3V		
		VCC=5V		
I_{IO}	Output current sunk by any I/O and control pin	VCC=3.3V		
		VCC=5V		
	Output current source by any I/Os and control pin	VCC=3.3V		
		VCC=5V		
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)			
	Injected current on any other pin(4)			
$SI_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)			

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 2. on page 76.
3. Positive injection is not possible on these I/Os. A negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to Voltage characteristics for the maximum allowed input voltagevalues.
4. A positive injection is induced by VIN>VDD while a negative injection is induced by VIN<VSS. IINJ(PIN) must never be exceeded. Refer to Voltage characteristics for the maximum allowed input voltagevalues.
5. When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

Thermal characteristics			
Symbol	**Ratings**	**Value**	**Unit**
TSTG	Storage temperature range		**°C**
TJ	Maximum junction temperature		**°C**

12.2 General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-			80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-			40	
f_{PCLK2}	Internal APB2 clock frequency	-			80	
V_{DD}	Standard operating voltage	-		2.5	5.5	V
$V_{DDA(1)}$	Analog operating voltage (ADC or OPA or PGA or CMP not used)	Must be the same potential as VDD (2)		2	5.5	
	Analog operating voltage (ADC or OPA or PGA or CMP used)			2.5	5.5	
V_{IN}	I/O input voltage	Standard IO		2	VDD5+0.5	V
		FT IO(3)	VDD=3.3V	2	5.5	
P_D	Power dissipation at TA = 105 °C (3)	LQFP64			444	mW
		LQFP80		-		

General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature	Maximum power dissipation	–40	105	°C
T_J	Junction temperature range		–40	105	

1.当使用 ADC 时，参见 12.18ADC 章节。
2.建议使用相同电源为 VDD 和 VDDA 供电，在上电和正常操作期间，VDD 和 VDDA 之间最多允许有 300mv 的差别。
3.如果 T_A 较低，只要 T_J 不超过 $T_J$max(参见第 1 节)，则允许更高的 PD 值。

12.3 Operating conditions PWR UP_DOW

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	VCC=3.3V	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
	V_{DD} rise time rate	VCC=5V	0	∞	
	V_{DD} fall time rate		20	∞	

12.4 Embedded reset and power

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)		2.23		V
		PLS[2:0]=000 (falling edge)		2.09		
		PLS[2:0]=001 (rising edge)		2.58		
		PLS[2:0]=001 (falling edge)		2.44		
		PLS[2:0]=010 (rising edge)		2.94		
		PLS[2:0]=010 (falling edge)		2.79		
		PLS[2:0]=011 (rising edge)		3.3		
		PLS[2:0]=011 (falling edge)		3.14		
		PLS[2:0]=100 (rising edge)		3.66		
		PLS[2:0]=100 (falling edge)		3.49		
		PLS[2:0]=101 (rising edge)		4.02		
		PLS[2:0]=101 (falling edge)		3.86		
		PLS[2:0]=110 (rising edge)		4.37		
		PLS[2:0]=110 (falling edge)		4.23		
		PLS[2:0]=111 (rising edge)		4.74		
		PLS[2:0]=111 (falling edge)		4.58		
$V_{PVDhyst}$(2)	PVD hysteresis	-		100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.83	1.86	1.87	V
		Rising edge	1.91	1.95	1.96	
$V_{PDRhyst}$(2)	PDR hysteresis	-		100		mV
$T_{RSTTEMPO}$(2)	Reset temporization	VCC=3.3V				ms
		VCC=5V	1	2.5	4.5	

1. The product behavior is guaranteed by design down to the minimum VPOR/PDR value.
2. Guaranteed by design.

12.5 Embedded internal reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < TA < +105 °C				**V**
		–40 °C < TA < +85 °C				
TS_vrefint(1)	ADC sampling time when reading the internal reference voltage					**us**
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	VDD=3.3V				**mV**
		VDD=5V				
T_{coeff}(2)	Temperature coefficient	-				**ppm/°C**

1.Shortest sampling time can be determined in the application by multiple interations.
2.Guaranteed by design.

12.6 Supply current

Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	fHCLK	Max(1)			Unit
				TA = 25 °C	TA = 105 °C	TA = 125 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled，VCC=3.3V	72 MHz				mA
		External clock(2), all peripherals disabled，VCC=3.3V	72 MHz				
		External clock(2), all peripherals enabled，VCC=5V	72 MHz				
		External clock(2), all peripherals disabled，VCC=5V	72 MHz				

1. Guaranteed based on test during characterization.
2. External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	fHCLK	Max(1)			Unit
				TA = 25°C	TA = 105 °C	TA=125 ℃	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled，VCC=3.3V	8 MHz				uA
		External clock(2), all peripherals disabled，VCC=3.3V					
		External clock(2), all peripherals enabled，VCC=5V	8 MHz				
		External clock(2), all peripherals disabled，VCC=5V					

1. Based on characterization, tested in production at VDD max, fHCLK max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when fHCLK > 8 MHz.

Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		MAX			Unit
			VCC = 3.3V	VCC = 5.0V	TA = 常温	TA =105 °C	TA = 125 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)						μA
		Regulator in Low-power mode, lowspeed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)						
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog OFF, lowspeed oscillator and RTC OFF(VCC=3.3V)						
		Low-speed internal RC oscillator and independent watchdog OFF, lowspeed oscillator and RTC OFF(VCC=5V)						

1. Typical values are measured at TA = 25 °C.
2. Guaranteed based on test during characterization.

Peripheral current consumption

Peripherals		µA/MHz
APB1 (up to 36 MHz)	DMA1	
	TIM2	
	TIM3	
	TIM4	
	SPI2	
	USART2	
	USART3	
	I2C1	
	I2C2	
	CAN1	
	WWDG	
	PWR	
	BKP	

Peripheral current consumption (continued)

Peripherals		µA/MHz
APB2 (up to 72 MHz)	APB2-Bridge	
	GPIOA	
	GPIOB	
	GPIOC	
	GPIOD	
	SPI1	
	USART1	
	TIM1	
	TIM8	
	OPA	
	CMP	
	ADC1(1)	
	ADC2(1)	

1. Specific conditions for measuring ADC current consumption: f HCLK = 56 MHz, f APB1 = f HCLK /2, f APB2 =f HCLK , f ADCCLK = f APB2/4 , When ADON bit in the ADCx_CR2 register is set to 1, a current consumption ofanalog part equal to 0.65 mA must be added for each ADC.

12.7 External clock

High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSE_ext	User external clock source frequency(1)	-	1	8	25	MHz
VHSEH	OSC_IN input pin high level voltage		0.7VDD	-	VDD	**V**
VHSEL	OSC_IN input pin low level voltage		VSS	-	0.3VDD	V
tw(HSE)	OSC_IN high or low time(1)		5	-	-	ns
tr(HSE) tf(HSE)	OSC_IN rise or fall time(1)		-	-	20	
Cin(HSE)	OSC_IN input capacitance(1)	-	-	5	-	pF

DuCy(HSE)	Duty cycle	-	45	50	55	%
IL	OSC_IN Input leakage current	VSS≤VIN≤VDD	-	-	±1	µA

1. Guaranteed by design.

HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fOSC_IN	Oscillator frequency	-	4	8	16	MHz
RF	Feedback resistor	-	-	1	-	KΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (RS)(3)	RS = 40 Ù	-	30	-	pF
i2	HSE driving current	4MHzVDD = 3.3 V	-	0.4	-	mA
		16MHzVDD = 5V	-	0.7	-	
gm	Oscillator transconductance	Startup	15	-	-	mA/V
tSU(HSE)(4)	startup time	VDD is stabilized	-	4	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed based on test during characterization.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. tSU(HSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

12.8 Internal clock source

High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	50	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-		
		Factory-calibrated(4)(5)	TA = –40 to 125 °C	-1.5	-	1.5	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HIS)}$(4)	HSI oscillator power consumption	-			100	200	µA

LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
fLSI(2)	Frequency	30 (-25%)	40	60 (+50%)	kHz
tsu(LSI)	LSI oscillator startup time			85	µs
IDD(LSI)(3)	LSI oscillator power consumption		0.6	2	µA

Low-power mode wakeup timings

Symbol	Parameter	min	max	Unit
tWUSLEEP	Wakeup from Sleep mode	-	1.8	µs
tWUST (1)	Wakeup from Stop mode (regulator in run mode)	-	3.6	µs

tWUSTDBY	Wakeup from Standby mode	-	50	

1. VDD = 5 V, TA = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed based on test during characterization.
4. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

12.9 PLL characteristics

Symbol	Parameter	Value			
		Min(1)	Typ	Max(1)	Unit
fPLL_IN	PLL input clock(2)	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
fPLL_OUT	PLL multiplier output clock	-	-	80	MHz
tLOCK	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter			300	ps

1. Guaranteed based on test during characterization.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f PLL_OUT

12.10 Memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
tprog	Byte programming time	TA = –40 to +105 °C				µs
tERASE	Sector erase time	TA = –40 to +105 °C				ms
	Chip erase time	TA = –40 to +105 °C				

1. Guaranteed by design.

Flash memory characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
IDD	Supply current	Read mode 40 MHz , VDD = 1.35 ~ 1.65V				mA
		Write / Erase modes VDD = 1.35 ~ 1.65V				
		Standby Current				µA
		Deep Standby Current				

1. Guaranteed by design.

Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
NEND	Endurance	TA = –40 to +105 °C				kcycles
tRET	Data retention	TA = 25 °C				Years
		TA = 85 °C				
		TA = 125 °C				

1. Guaranteed based on test during characterization.

12.11 EMC characteristics

EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
VFESD	Voltage limits to be applied on any I/O pin to induce a functional disturbance	VDD = 5 V, TA = +25 °C, fHCLK = 72 MHz conforms to IEC 61000-4-2	
VEFTB	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	VDD = 5V, TA = +25 °C, fHCLK = 72 MHz conforms to IEC 61000-4-4	

EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [fHSI/fHCLK] 72 MHz	Unit
SEMI	Peak level	VDD = 3.3 V, TA = 26 °C,55%RH,LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz		dBµV
			30 to 300 MHz		
			300 MHz to 1GHz		
			SAE EMI Level		-
		VDD = 5 V, TA = 26 °C,55%RH,LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz		dBµV
			30 to 300 MHz		
			300 MHz to 1GHz		
			SAE EMI Level		-

12.12 electrical sensitivity

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = +25 °C conforming to JESD22-A114			V
VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to ANSI/ESD STM5.3.1			

1. Guaranteed based on test during characterization

Electrical sensitivities

Symbol	Parameter	Conditions	Class	Maximum value(1)	Unit
LU	Static latch-up class	TA = +105 °C conforming to JESD78A	Level A		mA

12.13 IO port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage	All I/Os except BOOT0，DESIGN				V

		All I/Os except BOOT0，VDD=3.3V				
		All I/Os except BOOT0，VDD=5V				
VIH	High level input voltage	All I/Os except BOOT0，DESIGN				
		All I/Os except BOOT0，VDD=3.3V				
		All I/Os except BOOT0，VDD=5V				
Vhys	All IO Schmitt trigger voltage hysteresis(4)	-				mV
Ilkg	Input leakage current(6)	VIN=VDD				μA
		VIN = 0				
RPU	Weak pull-up equivalent resistor(7)	VDD=3.3V				kΩ
		VDD=5V				
RPD	Weak pull-down equivalent resistor(7)	VDD=3.3V				
		VDD=5V				
CIO	I/O pin capacitance	-				pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V DD +0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed based on test during characterization.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the serie s resistance is minimum (~10% order) .

Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VOL(1)	Output low level voltage for an I/O pin when 1 pins are sunk at same time	VDD=3.3V，IIO = -8 mA			V
		VDD=5V，IIO = -8 mA			
VOH(3)	Output high level voltage for an I/O pin when1 pins are sourced at same time	VDD=3.3V，Iio = +8 mA			
		VDD=5V，Iio = +8 mA			
VOL(1)(4)	Output low level voltage for an I/O pin when 1 pins are sunk at same time	VDD=3.3V I_{io} = -20 Ma			
		VDD=5V，IIO = -20 mA			
VOH(3)(4)	Output high level voltage for an I/O pin when 1 pins are sourced at same time	VDD=3.3V，IIO = +20 mA			
		VDD=5V，IIO = +20 mA			

I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	fmax(IO)out	Maximum frequency(2)	CL = 50pF, VDD = 3.3V			MHz
			CL = 50pF, VDD =5V			
	tf(IO)out	Output high to low level fall time	CL = 50 pF, VDD = 3.3V			ns
			CL = 50 pF, VDD =5V			
	tr(IO)out	Output low to high level rise time	CL = 50 pF, VDD = 3.3V			
			CL = 50 pF, VDD = 5V			
01	fmax(IO)out	Maximum frequency(2)	CL = 50 pF, VDD = 3.3V			MHz
			CL = 50 pF, VDD = 5V			
	tf(IO)out	Output high to low level fall time	CL = 50 pF, VDD = 3.3V			ns
			CL = 50 pF, VDD = 5V			
	tr(IO)out	Output low to high level rise time	CL = 50 pF, VDD = 3.3V			
			CL = 50 pF, VDD = 5V			
11	Fmax(IO)out	Maximum frequency(2)	CL =30 pF, VDD = 3.3V			MHz
			CL =30 pF, VDD =5V			
			CL = 50 pF, VDD = 3.3 V			
			CL = 50 pF, VDD =5V			
	tf(IO)out	Output high to low level fall time	CL =30 pF, VDD = 3.3V			ns
			CL =30 pF, VDD =5V			
			CL = 50 pF, VDD = 3.3 V			
			CL = 50 pF, VDD =5V			
	tr(IO)out	Output low to high level rise time	CL =30 pF, VDD = 3.3V			ns
			CL =30 pF, VDD =5V			
			CL = 50 pF, VDD = 3.3 V			
			CL = 50 pF, VDD =5V			
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-			ns

12.14 NRST

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL(NRST)(1)	NRST Input low level voltage	VDD=5V				V
		VDD=3.3V				
VIH(NRST) (1)	NRST Input high level voltage	VDD=5V				
		VDD=3.3V				
Vhys(NRST)	NRST Schmitt trigger voltage hysteresis	VDD=5V				V
		VDD=3.3V				
RPU	Weak pull-up equivalent resistor(2)					kΩ
VF(NRST)(1)	NRST Input filtered pulse	-				ns
VNF(NRST)	NRST Input not filtered pulse	-				ns

12.15 TIM Timer

Symbol	Parameter	Conditions	Min	Max	Unit
tres(TIM)	Timer resolution time	-			tTIMxCLK
		fTIMxCLK = 72 MHz			ns
fEXT	Timer external clock frequency on CH1 to CH4	-			MHz
		fTIMxCLK = 72 MHz			MHz
ResTIM	Timer resolution	-			bit
tCOUNTER	16-bit counter clock period when internal clock is selected	-			tTIMxCLK
		fTIMxCLK = 72 MHz			µs
tMAX_COUNT	Maximum possible count	-			tTIMxCLK
		fTIMxCLK = 72 MHz			s

12.16 Communications interfaces

I2C characteristics

Symbol	Parameter	Standard mode I2C(1)		Fast mode I2C(1)		Unit
		Min	Max	Min	Max	
tw(SCLL)	SCL clock low time					
tw(SCLH)	SCL clock high time					µs
tsu(SDA)	SDA setup time					
th(SDA)	SDA data hold time					
tr(SDA) tr(SCL)	SDA and SCL rise time					
tf(SDA) tf(SCL)	SDA and SCL fall time					ns
th(STA)	Start condition hold time					

tsu(STA)	Repeated Start condition setup time					µs
tsu(STO)	Stop condition setup time					ms
tw(STO:STA)	Stop to Start condition time (bus free)					ms
Cb	Capacitive load for each bus line					pF
tSP	Pulse width of spikes that are suppressed by the analog filter					ns

1.Design by Guarantee

SCL frequency (fPCLK1= 36 MHz.,VDD_I2C = 3.3 V、5V)(1)(2)

fSCL (kHz)	I2C_CCR value
	RP = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. RP = External pull-up resistance, fSCL = I2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
fSCK	SPI clock frequency	Master mode			MHz
1/tc(SCK)		Slave mode			
tr(SCK) tf(SCK)	SPI clock rise and fall time	Capacitive load: C = 30 pF			ns
Min SCK H/L	Mini SCK High / Low width	Master / Slave mode			ns
tsu(NSS)(1)	NSS setup time	Slave mode			ns
th(NSS)(1)	NSS hold time	Slave mode			
tw(SCKH)(1)	SCK high and low time	Master mode, fPCLK = 36 MHz, presc = 4			
tw(SCKL)(1)					
tsu(MI)(1)	Data input setup time	Master mode			
tsu(SI)(1)		Slave mode			
th(MI)(1)	Data input hold time	Master mode			
th(SI)(1)		Slave mode			
ta(SO)(1)	Data output access time	Slave mode, fPCLK = 20 MHz			
tdis(SO)(1)	Data output disable time	Slave mode			
tv(SO) (1)	Data output valid time	Slave mode (after enable edge)			
tv(MO)(1)	Data output valid time	Master mode (after enable edge)			
th(SO)(1)	Data output hold time	Slave mode (after enable edge)			
th(MO)(1)		Master mode (after enable edge)			

1.Design by Guarantee

USART Maximum Running Baud Rate

Interface	Maximum Baud Rate
USART1	
USART2 / USART3	

12.17 CAN

Refer to **I/O current injection characteristics** for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX)

Symbol	Parameter	Min	Max	Unit	Condition
fB	Bit timing			MHz	PCLK=8M,t(BS1)=4tq,t(BS2)=3tq, tq=tPCLK

12.18 ADC

ADC Chracteristics

	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	-				V
VREF+	Positive reference voltage	-				V
IVREF	Current on the VREF input pin	-				μA
fADC	ADC clock frequency	-				MHz
fs(2)	Sampling rate	-				MHz
fTRIG(2)	External trigger frequency	fADC = 12MHz				kHz
						1/fADC
VAIN (3)	Conversion voltage range					V
RAIN(2)	External input impedance	See Equation 1 and Table 47 for details				kΩ
RADC	Sampling switch resistance	-				kΩ
CADC(2)	Internal sample and hold capacitor	-				pF
t CAL(2)	Calibration time	fADC = 12 MHz				μs
		-				1/fADC
tlat(2)	Injection trigger conversion latency	fADC = 12 MHz				μs
		-				1/fADC
tlatr (2)	Regular trigger conversion latency	fADC = 12 MHz				μs
		-				1/fADC
t s(2)	Sampling time	fADC = 12 MHz				μs
		-				1/fADC
tSTAB(2)	Power-up time	-				μs
tCONV(2)	Total conversion time (including sampling time)	fADC = 12 MHz				μs
		-				1/fADC

1. Guaranteed based on test during characterization.
2. Guaranteed by design.

RAIN max for fADC = 12 MHz(1)

Ts (cycles)	tS (µs)	RAIN max (kΩ)
1.5	0.13	0.4
7.5	0.63	5.9
13.5	1.13	11.4
28.5	2.38	25.2
41.5	3.46	37.2
55.5	4.63	50
71.5	5.96	NA
239.5	19.96	NA

ADC accuracy - limited test conditions (1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	fPCLK2 = 72 MHz,			LSB
EO	Offset error	fADC = 12 MHz, RAIN < 10 kΩ, VDDA = 3 V to 5 V			
EG	Gain error	TA = 25 °C			
ED	Differential linearity error	Measurements made after			
EL	Integral linearity error	ADC calibration			

12.19 Temperature sensor

VCC=3.3V

Symbol	Parameter	Min	Typ	Max	Unit
TL	VSENSE linearity with temperature				°C
Avg_Slope	Average slope				mV/°C
V25	Voltage at 25 °C				V
Tstart	Startup time				µs
TS_temp	ADC sampling time when reading the temperature				µs

VCC=5V

Symbol	Parameter	Min	Typ	Max	Unit
TL	VSENSE linearity with temperature				°C
Avg_Slope	Average slope				mV/°C
V25	Voltage at 25 °C				V
Tstart	Startup time				µs
TS_temp	ADC sampling time when reading the temperature				µs

12.20 CMP

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD5}						V
I_{CC}	Operating current	VDD=3.3V,0				uA
		VDD=3.3V,1				
		VDD=3.3V,10				
		VDD=3.3V,11				
I_{CC}	Operating current	VDD=5V,0				uA
		VDD=5V,1				
		VDD=5V,10				
		VDD=5V,11				
V_{TH}	阈值电压	V_{TH}[3:0]				V
V_{OS}	Input offset voltage					mV
响应时间	VCM=VDD/2;	I_{CC}=100u, V(INP)-V(INN)=100mV				ns
		I_{CC}=100u, V(INP)-V(INN)=-100mV				
		I_{CC}=60u, V(INP)-V(INN)=100mV				
		I_{CC}=60u, V(INP)-V(INN)=-100mV				
		I_{CC}=38u, V(INP)-V(INN)=100mV				
		I_{CC}=38u, V(INP)-V(INN)=-100mV				
		I_{CC}=26u, V(INP)-V(INN)=100mV				
		I_{CC}=26u, V(INP)-V(INN)=-100mV				

$V_{HY(rise)}$	Signal low to high hysteresis	0				mV
		1				
		10				
		11				
$V_{HY(fall)}$	Signal high to low hysteresis	0				mV
		1				
		10				
		11				

12.21 OPA/PGA

OPA

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD5}	电源电压					V
ICC	Operating current	UINT GAIN，VCC=3.3V				uA
		UINT GAIN，VCC=5V				uA
CMIR	共模輸入电压					V
$V_{OS(IN)}$	输入失调电压	VCC=3.3V				mV
		VCC=5V				mV
AV	开环增益（条件）	C_{LOAD}=25pF				dB
GBW	单位增益带宽	CLOAD=25pF/ RLOAD=4K				MHz
PM	相位裕度	C_{LOAD}=25pF/ R_{LOAD}=4K				degree
SR	压摆率	C_{LOAD}=25pF				V/usec
T_{WAKEUP}	唤醒时间 0.1%精度（Unity gain）	VCC=3.3V,C_{LOAD}=25pF Current source wakeup				us
		VCC=3.3V,R_{LOAD}=4K Current source wakeup				
		VCC=3.3V,C_{LOAD}=25pF OPA wake up Current source ready				
		VCC=3.3V,R_{LOAD}=4K OPA wake up Current source ready				
		VCC=5V,C_{LOAD}=25pF Current source wakeup				

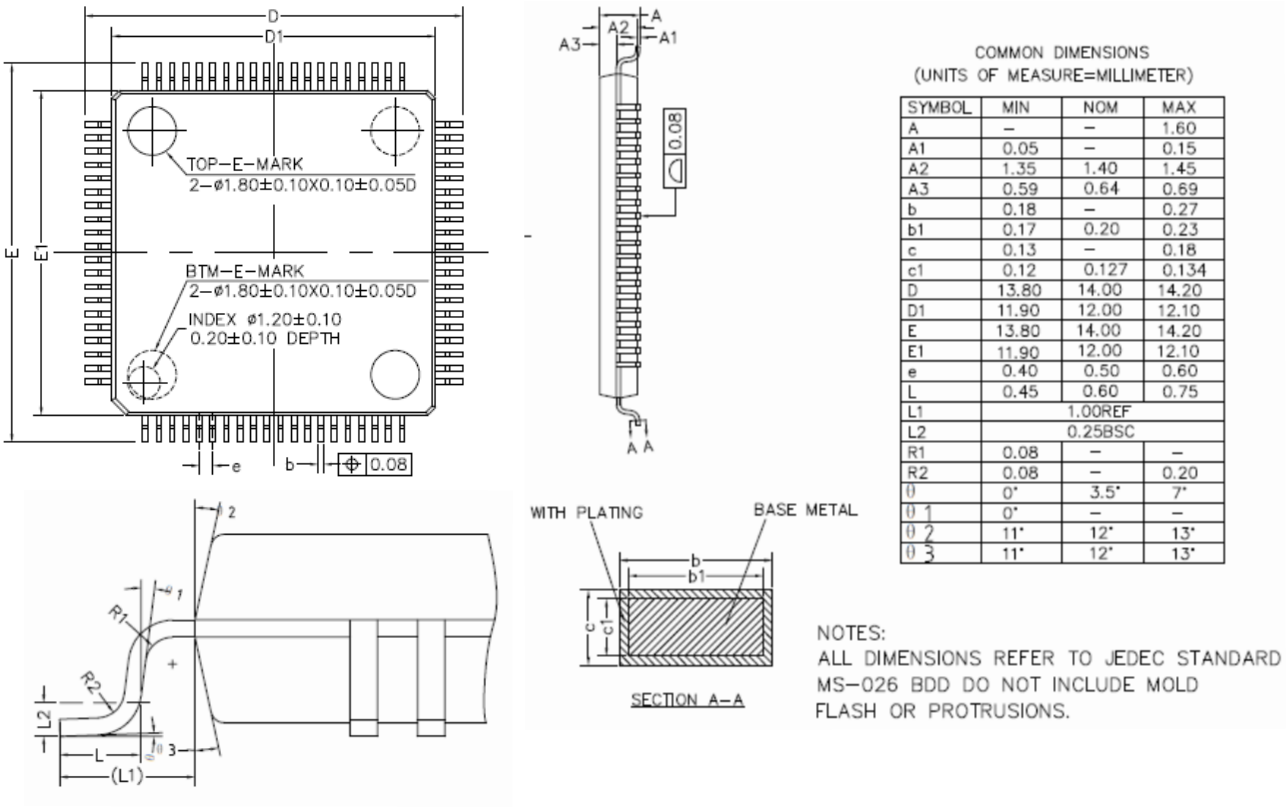
		VCC=5V,R_{LOAD}=4K Current source wakeup				
		VCC=5V,C_{LOAD}=25pF OPA wake up Current source ready				
		VCC=5V,R_{LOAD}=4K OPA wake up Current source ready				
R_{LOAD}	电阻性负载					K-ohm
C_{LOAD}	电容性负载					pF
$V_{OUT(SAT)}$	高饱和输出电压	R_{LOAD}=4K,输入 V_{DD5}				V
	低饱和输出电压	R_{LOAD}=4K,输入 0V				
$V_{N(referred-to-input)}$		@1KHz,R_{LOAD}=4K				nV/sqrt(Hz)
		@10KHz R_{LOAD}=4K				

PGA

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD5}	电源电压					V
ICC	Operating current	Gain=18，VCC=3.3V				mA
		Gain=18，VCC=5V				
CMIR	Common mode input range	-				V
V_{OLR}	Output range					V
R_{INDIF}	Differential Input impedance					K-ohm
T_{ST}	Settling time	1% of final value				ns
		(Cload=10pF)				
Av	Amplifier gain					V/V
PGA gain error	PGA gain error					%

封装图

LQFP80



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.